ABSTRACT OF THE DISCLOSURE

A CMOS logical circuit comprises two electric current paths each of which has circuits consisting of n-type and p-type transistors. In a circuit consisting of n-type or p-type transistors, one electric current path is provided with a circuit having the same construction as that of a circuit having an n-type transistor of a CMOS logical circuit outputting a logical operation result similar to that of this logical circuit, and the other electric current path is provided with a circuit having the same construction as that of a circuit having a p-type transistor of the CMOS logical circuit outputting a logical operation result similar to that of this logical circuit. In another circuit consisting of the other channel type, a gate electrode of the transistor provided on the one electric current path and that of the transistor provided on the other electric current path are connected to drain electrodes of the counterparts. According to the construction, the amplitude of an input signal can be made smaller than a supply voltage of the logical circuit.